

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a circuit pattern having a linear pattern, a perimeter
5 of the linear pattern per unit area being set in a specified range.

2. A semiconductor integrated circuit device comprising:

a circuit pattern having a linear pattern,

10 a dummy pattern being inserted in a region in which the circuit pattern is placed such that a sum perimeter of the linear pattern and the dummy pattern per unit area is set in a specified range.

15 3. The semiconductor integrated circuit device of claim 2, wherein the dummy pattern has a strip-like configuration.

4. A semiconductor integrated circuit device comprising:

20 a first circuit pattern having a first linear pattern and placed in a region in which a group of elements having a repetitive pattern are formed; and

a second circuit pattern having a second linear pattern and placed in a region in which components other than the group of elements are formed,

25 a dummy pattern being inserted in the region in which the second circuit pattern is placed such that a sum

perimeter of the first linear pattern, the second linear pattern, and the dummy pattern per unit area is equal to or less than a perimeter of the first linear pattern per unit area.

5 5. The semiconductor integrated circuit device of claim 4, wherein the group of elements are memories.

6. The semiconductor integrated circuit device of claim 4, wherein a perimeter of the dummy pattern per unit area is 70% or more of the perimeter of the first linear pattern per unit area.

7. A method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated circuit devices being common, the fabrication steps including the step of:

inserting a dummy pattern in a region in which the circuit pattern is placed such that a sum perimeter of the linear pattern and the dummy pattern per unit area is set in a specified range.

8. A method for fabricating a semiconductor integrated circuit device, the method comprising the steps of:

exposing each of a plurality of first regions of a semiconductor substrate to transfer a circuit pattern having a linear pattern onto the first region;

exposing each of a plurality of second regions of the semiconductor substrate other than the first regions to transfer a dummy pattern onto the second region; and

adjusting a ratio between the number of exposing shots for transferring the circuit pattern and the number of exposing shots for transferring the dummy pattern such that a sum perimeter of all the linear patterns transferred and all the dummy patterns transferred per unit area is set in a specified range.

9. A method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated circuit devices being common, the fabrication steps including the step of:

performing dry etching with respect to a target film while adjusting a dry etching condition in accordance with a perimeter of the linear pattern per unit area.

10. The method of claim 9, wherein the step of adjusting the dry etching condition includes the step of:

determining one dry etching condition when the perimeter of the linear pattern per unit area is within one range.

11. A method for fabricating a plurality of semiconductor integrated circuit devices each comprising a

circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated circuit devices being common, the fabrication steps including the step of:

- 5 forming a resist pattern corresponding to the linear pattern while adjusting a size of the resist pattern in accordance with a perimeter of the linear pattern per unit area.

12. A method for fabricating a plurality of semiconductor integrated circuit devices each comprising a circuit pattern having a linear pattern, at least one of fabrication steps for the semiconductor integrated circuit devices being common, the fabrication steps including:

- 15 a first step of forming a resist pattern corresponding to the linear pattern on a target film; and

 a second step of performing dry etching with respect to the target film by using the resist pattern as a mask, the second step including the step of:

20 using an etching gas having an effect of protecting a sidewall formed in the target film through the etching or forming an etching reaction product having the sidewall protecting effect,

 a processing method or a processing condition in at least one of the first and second steps being adjusted in accordance with a ratio between an area occupied by a group

25

of elements contained in the circuit pattern and having a repetitive pattern and an area of a region in which the circuit pattern is placed.

13. The method of claim 12, wherein the group of
5 elements are memories.

14. The method of claim 13, wherein the memories are DRAMs.

15. The method of claim 12, wherein the first step includes the step of:

10 increasing a size of the resist pattern as the ratio increases.

16. The method of claim 12, wherein the second step includes the step of:

15 determining an etching condition such that the sidewall protecting effect increases as the ratio increases.